CLAIMS

We claim:

1. An electronic assembly comprising:

a substrate;

a die;

a plurality of interconnections between the substrate and die;

wherein respective ones of the interconnections include a relatively low melting temperature and yield strength solder on the die, a relatively higher melting temperature and electrically conductive material on the substrate, and a soldered joint connecting the solder to the electrically conductive material.

2. The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material on the substrate is formed as a standoff extending above a surface of the substrate.

3. The electronic assembly according to claim 2, wherein the top surface of the standoff is wetted by the solder to form the soldered joint.

4. The electronic assembly according to claim 2, wherein the standoff is a bump in the form of a column or stud.

5. The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material is copper.

6. The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material is solder having a melting temperature higher than the melting temperature of the solder on the die.

7. The electronic assembly according to claim 1, wherein the die has an inter layer dielectric material under the interconnections.

8. The electronic assembly according to claim 7, wherein the inter layer dielectric material has cohesive and adhesive strengths at least about an order of magnitude less than those of carbon doped oxide inter layer dielectric material.

9. The electronic assembly according to claim 1, wherein the coefficient of thermal expansion of the substrate is at least 15 ppm/°C and the coefficient of thermal expansion of the die is at least 2.7 ppm/°C less than that of the substrate.

10. The electronic assembly according to claim 1, wherein the coefficient of thermal expansion of the substrate is more than two times greater than the coefficient of thermal expansion of the die.

11. A semiconductor package comprising:

a package substrate having a coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of relatively high melting temperature and electrically conductive contact members on the substrate;

a die having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than that of the substrate, a front side of the die having a plurality of relatively lower yield strength solder connections thereon, the die being located on the substrate with the solder connections connected to the respective ones of the contact members by soldered joints electrically coupling the die to the substrate.

12. The semiconductor package according to claim 11, wherein the coefficient of thermal expansion of the substrate is more than twice that of the die.

13. The semiconductor package according to claim 12, wherein the contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements.

14. The semiconductor package according to claim 13, wherein the standoff elements are non-melting at the solder liquidous temperature.

15. The semiconductor package according to claim 13, wherein the standoff elements are copper bumps.

16. The semiconductor package according to claim 13, wherein the soldered joints each comprise solder on the die which is wetted onto a surface of a contact member of the substrate to form the soldered joint.

17. The semiconductor package according to claim 11, wherein the die has an inter layer dielectric material under the solder connections thereon.

18. The semiconductor package according to claim 17, wherein the inter layer dielectric material has cohesive and adhesive strengths at least about on an order of magnitude less than those of carbon doped oxide inter layer dielectric material.

19. A method of interconnecting a die and substrate to one another for reduced die stresses, the method comprising:

providing a relatively low melting temperature and yield strength solder on a die and a relatively higher melting temperature and electrically conductive material contact member on a substrate; and

forming a soldered joint connecting the solder to the electrically conductive material.

20. The method according to claim 19, wherein the contact member is formed as a standoff extending above a surface of the substrate.

21. The method according to claim 20, wherein the solder is wetted on the top surface of the standoff to form the soldered joint.

22. The method according to claim 19, wherein the solder is provided over an inter layer dielectric material in the die.

23. The method according to claim 22, wherein the inter layer dielectric material has cohesive and adhesive strengths at least about an order of magnitude less than those of carbon doped oxide inter layer dielectric material.

24. The method according to claim 19, wherein the coefficient of thermal expansion of the substrate is at least 15 ppm/°C and the coefficient of thermal expansion of the die is at least 2.7 ppm/°C less than that of the substrate.

25. The method according to claim 19, wherein the soldering includes separately heating the die and solder to at least a soldering temperature and thereafter contacting the solder with the contact member on the substrate for forming the soldered joint.

26. The method according to claim 25, further comprising separately heating the substrate to a temperature substantially lower than the soldering temperature before contacting the solder on the die with the contact member on the substrate to form the soldered joint.